REMARKS

The Official Action mailed February 21, 2002 has been received and its contents carefully noted. This Preliminary Amendment and remarks are submitted in response to this Official Action and further to the *Request for Continued Examination* filed June 21, 2002.

Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on September 5, 2000, February 15, 2001, March 15, 2001 and August 15, 2001. However, Applicant has no record of receiving acknowledgement of the Information Disclosure Statements filed on March 22, 2001 and November 2, 2001. Consideration and return of initialed copies of the PTO 1449 forms is respectfully requested.

Initially, Applicant notes that the present application claims priority to U.S. Application Serial Number 07/811,063 filed December 20, 1991. The '063 application is a continuation-in-part (CIP) of Application Serial Number 08/293,201, which in turn claims priority to Application Serial Number 07/673,821 filed March 22, 1991. MPEP 201.08 provides that unless the filing date of the earlier '821 application is actually needed, for example, in the case of an interference or to overcome a reference, then there is no need for the Office to make a determination as to whether the '821 application discloses the present invention in the manner provided by the first paragraph of 35 U.S.C. 112. Thus, it is understood that the examination will be conducted based on the filing date of the '063 application (December 20, 1991) unless an intervening reference is located, at which time the Examiner will consider whether the '821 application meets the requirements of 35 USC 112, first paragraph.

Claims 21-41 and 43-78 were pending in the present application. Claims 21-41, 43-44, 48, 53, 57-59, 64 and 66 have been amended herewith and new claims 79-90 have been added to recite additional protection to which Applicant is entitled. Thus, claims 21-41 and 43-90 are now pending in the present in application, of which claims 21-32 and 41 are independent. For the reasons set forth in detail below, these claims are believed to be in condition for allowance and favorable consideration is requested.

The Official Action rejects claims 21-41 and 43-66 under the doctrine of obviousness-type double patenting based on claims 1-46 of U.S. Patent No. 6,023,075.

The Official Action further rejects claims 67-78 under 35 U.S.C. 101 as claiming the same invention as that of claims 1-45 of U.S. Patent No. 6,023,075 (i.e. statutory double patenting). Applicant respectfully requests that these rejections be held in abeyance until an indication of allowability has been received, at which time a complete response will be made to any remaining double patenting objections.

The Official Action next rejects claims 21-41, 43-44, 49, 52-53, 56 and 61-78 as obvious based on the combination of U.S. Patent 3,821,781 to Chang, U.S. Patent 5,656,826 to Misawa and JP 60-245173 to Yamazaki. Also, claims 21-41, 43-56 and 61-78 are rejected as obvious based on the combination of Chang, Misawa, Yamazaki and U.S. Patent 4,703,552 to Baldi. Claims 21-41 and 43-78 are further rejected as obvious based on the combination of Chang, Misawa, Yamazaki, Baldi, JP 2-234134 to Sumiyoshi and the article *An Active-Matrix LCD with Integrated Driver Circuits Using a-Si TFTs* by Akiyama.

As stated in MPEP § 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Referring to page 3 of the Detailed Action, in response to Applicant's previous remarks, the Official Action asserts that "leveling film" 84, 95 of Misawa clearly covers

both areas of transistors and cites column 6, lines 61-64 in support of this assertion. Applicant respectfully disagrees. Misawa never teaches or suggests that the films 84 and 95 are "leveling." Rather, Misawa merely teaches that insulating layers 78, 79, 82 and 84 can be formed of silicon oxides such as SiO_2, silicon nitride and the like (see column 6, lines 38-39). Although the Official Action mailed October 18, 2001 asserts that the insulating film 84, 95 "can function or be labeled as a 'leveling film'" the fact remains that the reference itself fails to disclose such a function or label. Thus, Applicants contend that layers 84 and 95 of Misawa cannot fairly be construed as leveling layers without a further showing that these layers act as leveling layers.

With respect to Akiyama, it should be noted that in Akiyama the passivation (polyimide) layer is located over the pixel electrode while in the present invention the pixel electrode is formed over the leveling layer. This limitation is recited in each of the independent claims as amended herewith. One feature of the present invention is to provide a leveled upper surface for pixel electrodes. Akiyama, however, is not directed to this purpose. Rather, as clearly shown in the drawings of Akiyama, there is a large step between the pixel electrode and the polyimide passivation layer. Therefore, the entire structure of Akiyama is different from the structure of the present invention as recited in the present claims.

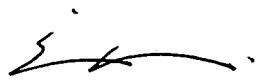
With respect to Sumiyoshi, it is asserted that Sumiyoshi fails to teach the specific structure of the transistor of the peripheral driving circuit. One feature of the present invention resides in that the thin film transistors of the peripheral driving circuit are manufactured through the same process as the thin film transistors of the pixel portion as taught on page 5, lines 2-7 of the present specification, for example, and thus have basically the same crystalline structure. In Sumiyoshi, it appears that the pixel TFTs are made of polysilicon while the peripheral driving circuit TFTs are made of single crystalline silicon. Therefore, it is respectfully submitted that the present invention can be distinguished from Sumiyoshi for at least this reason.

It is respectfully submitted that the prior art references, whether taken alone or in combination, fail to teach or suggest all the claim limitations and that a *prima facie* case of obviousness cannot be maintained. It is respectfully submitted that the prior art of record fails to disclose or suggest a device having at least a leveling layer formed over

pixel TFTs and driver circuit TFTs that are formed from the same process, and a pixel electrode formed over the leveling layer. Absent a disclosure or suggestion in the references of record, alone or in combination, it is respectfully submitted that a *prima facie* case of obviousness cannot be maintained and favorable reconsideration is respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 21-41, 43-44, 48, 53, 57-59, 64 and 66 as follows:

21. (Twice Amended) An active matrix display device having a pixel portion and a driver circuit portion, said driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; [and]

a leveling film covering each of said thin film transistors in both of the pixel portion and a part of the driver circuit [portion,] portion;

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the driver circuit portion are formed by a same process simultaneously.

22. (Twice Amended) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; [and]

a leveling film covering each of said thin film transistors in both of the pixel portion and the shift [register,] register; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the shift register are formed by a same process simultaneously .

23. (Twice Amended) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; [and]

a leveling film covering each of said thin film transistors in both of the pixel portion and the [inverter,] inverter; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the inverter are formed by a same process simultaneously.

24. (Twice Amended) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; [and]

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked [inverter,] inverter; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the clocked inverter are formed by a same process simultaneously.

25. (Twice Amended) An active matrix display device having a pixel portion and a driver circuit portion, said driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and a gate electrode adjacent to said gate insulating film; [and]

a leveling film covering each of said thin film transistors in both of the pixel portion and a part of the driver circuit [portion,] portion; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein a laser Raman spectroscopy of the crystalline semiconductor islands of the thin film transistors of the pixel portion and the driver circuit portion exhibits a peak shifted to a lower frequency side as compared with a peak of single crystal silicon.

26. (Twice Amended) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; [and]

a leveling film covering each of said thin film transistors in both of the pixel portion and in the shift [register,] register; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the shift register are formed by a same process simultaneously.

27. (Twice Amended) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; [and]

a leveling film covering each of said thin film transistors in both of the pixel portion and the [inverter,] inverter; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 cm2/V·sec or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 cm2/V·sec or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the inverter are formed by a same process simultaneously.

28. (Twice Amended) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; [and]

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked [inverter,] inverter; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the clocked inverter are formed by a same process simultaneously .

29. (Twice Amended) An active matrix display device having a pixel portion and a driver circuit portion, said driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; [and]

a leveling film covering each of said p-channel and n-channel thin film transistors in both of the pixel portion and a part of the driver circuit [portion,] portion; and

a pixel electrode formed over the leveling film,

[wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,]

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than 7×10^{19} cm^{-3}.

30. (Twice Amended) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; [and]

a leveling film covering each of said thin film transistors in both of the pixel portion and the shift [register,] register; and

a pixel electrode formed over the leveling film,

[wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,]

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

31. (Twice Amended) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; [and]

a leveling film covering each of said thin film transistors in both of the pixel portion and the [inverter,] inverter; and

a pixel electrode formed over the leveling film,

[wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,]

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

32. (Twice Amended) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; [and]

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked [inverter,] inverter; and

a pixel electrode formed over the leveling film,

[wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,]

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

33. (Amended) A [circuit] semiconductor device according to any one of claims 22-24, 26-28, and 30-32 wherein said semiconductor is silicon.

34. (Amended) A [circuit] semiconductor device according to any one of claims 22-24, 26-28, and 30-32 wherein said gate electrode comprises crystalline silicon doped with phosphorus.

35. (Amended) A [circuit] semiconductor device according to any one of claims 22-24, 26-28, and 30-32 wherein said gate electrode is a multilayer film of crystalline silicon doped with phosphorus and a metal film thereon, said metal comprising at least a material selected from the group consisting of Mo, W, $MoSi_2$, and Wsi_2.

36. (Amended) A [circuit] semiconductor device according to any one of claims 22-24, 26-28, and 30-32 wherein said semiconductor island comprises oxygen at a concentration not higher than $1x10^{19}$ cm^{-3}.

37. (Amended) A [circuit] semiconductor device according to any one of claims 22-24, [26-28,] and 30-32 wherein said crystalline semiconductor island exhibits a Raman peak shifted to a lower frequency side from 522 cm^{-1}.

38. (Amended) A [circuit] semiconductor device according to claim 34 wherein said phosphorus doped in said crystalline silicon is at a concentration of $1x10^{21}$ to $5x10^{21}$ cm^{-3}.

39. (Amended) A [circuit] semiconductor device according to any one of claims 22-24, 26-28, and 30-32 wherein said source and drain regions of n-channel thin film transistor are introduced with phosphorus at a dose of $1x10^{15}$ to $5x10^{15}$ cm^{-3}.

40. (Amended) A [circuit] semiconductor device according to any one of claims 22-24, 26-28, and 30-32 wherein said semiconductor island has a thickness of 500-[500] 5000 Å.

41. (Twice Amended) An active matrix display device including a pixel portion and a driver circuit portion comprising:

a plurality of pixel electrodes formed on an insulating surface;

a first plurality of thin film transistors being formed in the pixel portion on said insulating surface and being connected to said pixel electrodes;

a second plurality of thin film transistors being formed in the driver circuit portion on said insulating surface, said second plurality of thin film transistors including at least one pair of complementary p-channel and n-channel thin film transistors; and

a leveling film covering both of the first and second plurality of thin film transistors in the pixel portion and a part of the driver circuit portion, wherein said pixel electrodes are formed over the leveling film,

wherein said second plurality of thin film transistors in said driver circuit include channel semiconductor layers having at least one of an electron mobility 15 $cm^2/V \cdot sec$ or more and a hole mobility of 10 $cm^2/V \cdot sec$ or more, and

wherein each of said channel semiconductor layers has a thickness of 5000 Å or less.

43. (Amended) A device according to claim 41 [or 42] wherein said semiconductor is silicon.

44. (Amended) A device according to claim 41 [or 42] wherein each of the first and second plurality of said thin film transistors comprises a gate electrode formed over said channel semiconductor layers having a gate insulating film therebetween.

48. (Amended) A device according to claim 41 [or 42] wherein said channel semiconductor layers exhibit a Raman peak shifted to a lower frequency side from 522 cm^{-1}.

53. (Amended) A device according to any one of claims 21, [25,] and 29 wherein said crystalline semiconductor island exhibits a Raman peak shifted to a lower frequency side from 522 cm^{-1}.

57. (Amended) A [circuit] semiconductor device according to any one of claims 22-24, 26-28, and 30-32, wherein said leveling film comprises an organic resin.

58. (Amended) A [circuit] semiconductor device according to claim 57, wherein said organic resin is a transparent polyimide resin.

59. (Amended) A device according to any one of claims 21, 25, 29, and 41 [and 42], wherein said leveling film comprises an organic resin.

61. (Amended) A [circuit] semiconductor device according to any one of claims 22-24, 26-28, and 30-32, wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 200 $cm^2/V.sec$ or less and said semiconductor island of n-channel thin film transistor has a electron mobility in the range of 300 $cm^2/V.sec$ or less.

64. (Amended) A [circuit] semiconductor device according to any one of the claims 22-24, and 30-32, wherein said n-channel thin film transistor has an approximately same absolute value of a threshold voltage as said p-channel thin film transistor.

66. (Amended) A [circuit] semiconductor device according to claim 35 wherein said phosphorus doped in said crystalline silicon is at a concentration of $1x10^{21}$ to $5x10^{21}$ cm^{-3}.